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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,123	12/29/2000	Calvin Guey	JCLA6706	8730

7590 09/21/2004

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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,123	GUEY ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2, 6, and 9-12 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 7/27/2004.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of coprocessors must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 2 is objected to because of the following informalities: In line 2, insert a colon after "comprising". In line 4, replace "includes" with --include--. In line 9, the phrase "one of addressing modes" is of improper grammar and should therefore be modified. In line 17, replace "number of word data" with --a number of word data--. Appropriate correction is required.

6. Claim 6 recites the limitation "the value" in line 5. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 6 recites the limitation "the coprocessor indicating field" in line 5. There is insufficient antecedent basis for this limitation in the claim as only an indicating field is previously mentioned.

8. Claim 6 recites the limitation "the coprocessor memory access instruction" in line 6. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 6 is objected to because of the following informalities: In line 9, replace "number of word data" with --a number of word data--. Also, remove the space between "activated" and the period at the end of the claim. Appropriate correction is required.

10. Claim 9 recites the limitation "the computer" in line 3. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 9 recites the limitation "the number of data words" in line 4. There is insufficient antecedent basis for this limitation in the claim.

12. Claims 10 and 11 are unclear because they claim that the indicating field is either a coprocessor number field or a register number field. However, claim 9 (parent of claims 10 and 11) clearly sets forth that the indicating field is both a coprocessor number field and a coprocessor register field. Consequently, it is not clear to the examiner how the indicating field of claims 10 and 11 can be only one of a coprocessor number field and register field when in fact it is both.

13. Claim 12 recites the limitation "the coprocessor memory instruction" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

14. Claim 12 is objected to because of the following informalities: In line 3, insert --the-- before "coprocessor number field". Appropriate correction is required.

Claim Rejections - 35 USC § 101

15. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

16. Claims 9-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. More specifically, applicant claims an instruction format having multiple fields, which is nonfunctional, descriptive material. "Apart from the utility requirement of 35 U.S.C. 101, usefulness under the patent eligibility standard requires significant

functionality to be present to satisfy the useful result aspect of the practical application requirement. See Arrhythmia, 958 F.2d at 1057, 22 USPQ2d at 1036. Merely claiming nonfunctional descriptive material stored in a computer-readable medium does not make the invention eligible for patenting. For example, a claim directed to a word processing file stored on a disk may satisfy the utility requirement of 35 U.S.C. 101 since the information stored may have some "real world" value. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application. (MPEP 2106)." The examiner asserts that a useful result is not achieved by merely reading a format but instead by executing an actual instruction of the claimed format.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 2, 6, and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over York et al., U.S. Patent No. 6,002,882 (as applied in the previous Office Action and herein referred to as York) in view of Zolnowsky et al., U.S. Patent No. 4,729,094 (as previously disclosed and herein referred to as Zolnowsky).

19. Referring to claim 2, York has taught an apparatus for coprocessor data access control, comprising:

a) a central processing unit, for executing central processing unit instructions to perform data processing, wherein the central processing unit instructions includes a plurality of coprocessor memory access instructions. See column 1, line 66, to column 2, line 67.

b) a memory unit, coupled to the central processing unit, for storing data words. See column 2, lines 3-4.

c) a coprocessor, coupled to the central processing unit and the memory unit, for accessing and processing the data words stored in the memory unit by one of addressing modes under control of the coprocessor memory access instructions executed by the central processing unit. See column 2, lines 5-10.

d) the coprocessor memory access instruction having an indicating field, wherein the indicating field of the coprocessor memory access instruction includes a coprocessor register field for storing information about specific registers to be used. See column 63, lines 5-28 and note the "basereg" and "8_bit_offset" fields. These two combined are referred to as the "coprocessor register field" which specifies the first of a specified number of registers to be involved in the memory access.

e) York has not taught a plurality of coprocessors, each of the coprocessors coupled to the CPU and memory unit, and the indicating field including a coprocessor number field for storing information about a specific coprocessor to be activated, wherein the coprocessor number field determines one of the coprocessors to be activated. However, Zolnowsky has taught the concept of multiple coprocessor system in which a CPU may communicate with a given processor by

specifying a coprocessor number in a coprocessor number field of an instruction. See Fig.3 and note the general instruction, for instance, includes a CP=ID field (coprocessor ID). Also, see column 4, lines 9-11, and column 5, lines 32-40. A person of ordinary skill in the art would have recognized that multiple coprocessors are capable of performing more combined work than just a single coprocessor. In addition, if multiple coprocessors are implemented, a coprocessor number field is needed so that the main processor is able to coordinate execution with a given coprocessor, thereby allowing the system's coprocessors to perform a variety of tasks simultaneously. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify York such that multiple coprocessors exist instead of a single coprocessor and that instructions include a coprocessor number field for selecting one of the multiple coprocessors.

f) York in view of Zolnowsky has further taught that a number of word data that needs to be transmitted is determined by the coprocessor number field and the coprocessor register field. See column 63, lines 5-28, and the abstract of York. Note that in a memory access associated with a specific coprocessor, the coprocessor must be identified (via coprocessor number field) as well as the number of registers (via the 8_bit_offset field shown in column 63, lines 5-28, which is part of the overall register field).

20. Referring to claim 6, York has taught a coprocessor data access control method, comprising the steps of:

a) providing an instruction having an indicating field. See column 63, lines 5-28. Note that all parts of an instruction indicate something and therefore are indicating fields.

b) accessing a memory unit by a specified coprocessor according to the value in the indicating field. See column 2, lines 5-10.

c) wherein the indicating field of the coprocessor memory access instruction includes a coprocessor register field for storing information about specific registers to be used. See column 63, lines 5-28 and note the "basereg" and "8_bit_offset" fields. These two combined are referred to as the "coprocessor register field" which specifies the first of a specified number of registers to be involved in the memory access.

d) York has not taught that the indicating field including a coprocessor number field for storing information about a specific coprocessor to be activated, wherein the coprocessor number field determines one of a plurality of coprocessors to be activated. However, Zolnowsky has taught the concept of multiple coprocessor system in which a CPU may communicate with a given processor by specifying a coprocessor number in a coprocessor number field of an instruction. See Fig.3 and note the general instruction, for instance, includes a CP=ID field (coprocessor ID). Also, see column 4, lines 9-11, and column 5, lines 32-40. A person of ordinary skill in the art would have recognized that multiple coprocessors are capable of performing more combined work than just a single coprocessor. In addition, if multiple coprocessors are implemented, a coprocessor number field is needed so that the main processor is able to coordinate execution with a given coprocessor, thereby allowing the system's coprocessors to perform a variety of tasks simultaneously. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify York such that multiple coprocessors exist instead of a single coprocessor and that instructions include a coprocessor number field for selecting one of the multiple coprocessors.

e) York in view of Zolnowsky has further taught that a number of word data that needs to be transmitted is determined by the coprocessor number field and the coprocessor register field. See column 63, lines 5-28 and the abstract of York. Note that in a memory access associated with a specific coprocessor, the coprocessor must be identified (via coprocessor number field) as well as the number of registers (via the 8_bit_offset field shown in column 63, lines 5-28, which is part of the overall register field).

21. Referring to claim 9, York has taught an instruction format recorded on a computer readable medium for a coprocessor data access control (column 63, lines 5-28), wherein the instruction format includes an indicating field (all fields of the instruction are indicating fields).

a) York has not taught that while the instruction format is read by the computer, a coprocessor number determines one of a plurality of coprocessors to be activated. However, Zolnowsky has taught the concept of multiple coprocessor system in which a CPU may communicate with a given processor by specifying a coprocessor number in a coprocessor number field of an instruction. See Fig.3 and note the general instruction, for instance, includes a CP=ID field (coprocessor ID). Also, see column 4, lines 9-11, and column 5, lines 32-40. A person of ordinary skill in the art would have recognized that multiple coprocessors are capable of performing more combined work than just a single coprocessor. In addition, if multiple coprocessors are implemented, a coprocessor number field is needed so that the main processor is able to coordinate execution with a given coprocessor, thereby allowing the system's coprocessors to perform a variety of tasks simultaneously. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify York such that

multiple coprocessors exist instead of a single coprocessor and that instructions include a coprocessor number field for selecting one of the multiple coprocessors.

b) York in view of Zolnowsky has further taught that a number of data words being accessed to or from a memory unit is determined by the coprocessor number and a register number specified in the indicating field only. See column 63, lines 5-28, and the abstract of York. Note that in a memory access associated with a specific coprocessor, the coprocessor must be identified (via coprocessor number field) as well as the number of registers (via the 8_bit_offset field shown in column 63, lines 5-28).

22. Referring to claim 10, York in view of Zolnowsky has taught an instruction format as described in claim 9. York in view of Zolnowsky has further taught that the indicating field of the instruction format is a coprocessor number field. Clearly, if the indicating field (all of the instruction fields) specifies a coprocessor number, as taught by Zolnowsky, then the indicating field is a coprocessor number field.

23. Referring to claim 11, York in view of Zolnowsky has taught an instruction format as described in claim 9. York in view of Zolnowsky has further taught that the indicating field of the instruction format is a coprocessor register field. Clearly, if the indicating field (all of the instruction fields) specifies a coprocessor register, as taught by York (see column 63, lines 5-28, and note the "basereg" field, for instance), then the indicating field is a coprocessor register field.

24. Referring to claim 12, York in view of Zolnowsky has taught an instruction format as described in claim 9. York in view of Zolnowsky has further taught that the indicating field of the instruction format includes a coprocessor number field and a coprocessor register field, wherein the coprocessor number field is used for storing information about a specific

coprocessor to be activated, and the coprocessor register field is used for storing information about specific registers to be used in the data processing. Again, Zolnowsky has taught identifying one of multiple coprocessors via coprocessor number field in an instruction. And, York has taught "basereg" and "8_bit_offset" fields, which combine to form the overall "coprocessor register field". See column 63, lines 5-28. This register field specifies the first of a specified number of registers to be involved in the memory access.

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
September 17, 2004

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